IR-1444 DIV (2-2480)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Patent Application of	Confirmation No. 7041
Milton J. Boden, Jr. et al.	Date: December 3, 2008
Serial No.: 09/691,083	Group Art Unit: 2823
Filed: October 18, 2000	Examiner: G.R. Fourson III

For: P CHANNEL RADHARD DEVICE WITH BORON DIFFUSED P-TYPE POLYSILICON GATE

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF PURSUANT TO 37 C.F.R. §41.37

Sir:

This appeal is from the Final Office Action dated July 3, 2008.

I. REAL PARTY IN INTEREST

The real party in interest in the above-identified application is:

International Rectifier Corporation
233 Kansas Street
El Segundo, California 90245

II. RELATED APPEALS AND INTERFERENCES

The applicant(s), the assignee(s) and the undersigned attorneys are not aware of any related appeals and interferences.

III. STATUS OF CLAIMS

Claims 1, 3-7, 9 and 11-13 are pending and on appeal herein.

Claims 2, 8, 10 and 14-31 have previously been canceled.

IV. STATUS OF AMENDMENTS

All amendments have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In a Mosgated device that is deployed in a high radiation environment, e.g. outer space, the effects of ionizing radiation can accumulate over time, resulting in device degradation. (Spec., page 1, lines 17-21). Also, a single heavy ion strike (single event effect or SEE) can lead to catastrophic failure. (Spec., page 1, lines 21-22). MOSgated power devices are particularly susceptible to these problems because of their large depletion volumes and large device areas. (Spec., page 1, line 17 - page 2, line 3).

Radiation hardened power MOSFETs, and other MOS gated devices designed for use in space or other high radiation environments have the conflicting design requirements of resisting damage caused by high doses of ionizing radiation on the one hand and of resisting damage due to SEE. (Spec., page 2, lines 4-10). Specifically, a thin gate oxide is desired to resist high radiation environments, while a relatively thick gate oxide is desired to prevent SEE. (Spec., page 2, line 14, page 3, line 4).

More specifically, it is known that after exposure to a large total dose of ionizing radiation a positive charge will build up in or at the gate oxide, which causes a shift in the threshold voltage of the device. (Spec., page 2, lines 14-17). Further, there is an increase of interface traps at the silicon/gate oxide boundary. (Spec., page 2, lines 17-19). Conventional thinking is that both of these effects are reduced by using a thinner gate oxide, for example, one having a thickness of less than about 900Å. (Spec., page 2, lines 14-21).

When a single, high energy charged particle passes into or through the silicon body of a MOSgated device it generates a large number of electron-hole pairs in the depletion region of the device some of which gather at the gate oxide, resulting in a high potential across the gate oxide (spec., page 2, line 22 - page 3, line 2). This event is referred to as an SEE. To prevent failure due to an SEE the conventional solution was a gate oxide thicker than about 1300Å. (Spec., page 2, lines 22 - page 3, line 4).

Contrary to the conventional thinking, however, the inventors have discovered that a P channel power MOSFET having a radiation hardened gate oxide that is less than 1000Å thick,

(spec., page 11, lines 14-15), can maintain a predetermined threshold voltage (i.e. resist voltage shift) at a high total irradiation dose, and also maintain SEE withstand capability. (Spec., page 17, line 22 - page 18, line 3). That is, it was generally understood that to obtain sufficient resistance to damage due to SEE the gate oxide must be made at least thicker than 1300 Å. (Spec., page 2, line 22, page 3, line 4). However, as demonstrated by the data in the application, (see spec., page 17, line 3 to page 18, line 3; see also Figure 14) a device according to the present invention is capable of withstanding damage due to SEE, despite having a thinner than 1300 Å gate oxide.

More specifically, a device according to the present invention, which includes a gate oxide that is less than 1000Å thick, is capable of resisting a threshold shift to -5 that may be caused due to an SEE as well as due to total dose radiation. (Spec., page 6, lines 13-16; spec., page 16, line 25 - page 17, line 2; spec., page 17, lines 23-25).

Claim 1, therefore, calls for the following combination of features:

> 1. A P-channel MOS gated device which is resistant to single event radiation failure and having improved total dose radiation resistance; said device comprising:
>
> a P-type substrate having parallel upper and lower surfaces;
>
> a plurality of laterally spaced N-type body regions extending from said upper surface into said substrate;
>
> at least one respective P-type source region formed in each of said body regions in said upper surface of said substrate and defining a respective channel region in said upper surface in said N-type body region;
>
> a gate electrode comprised of polysilicon implanted with p-type dopants disposed atop and insulated from said channel region and operable to invert said channel region in response to ~~the~~ application of a suitable gate voltage to said gate electrode said gate electrode being insulated from said channel region by a gate oxide layer comprising silicon dioxide, said gate oxide layer being comprised of radiation hardened silicon dioxide and less than 1000Å thick;

an interlayer oxide disposed over each gate electrode and having tapered profile portions each aligned with a respective P-type source region; and

a source electrode disposed atop said upper surface and connected to said at least one P-type source region;

wherein said gate oxide is capable of withstanding damage due to total radiation dose and capable of withstanding damage due to a single event effect that may cause a threshold voltage shift to -5 volts.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1, 3-7, 9 and 11-13 were properly rejected as failing to comply with 35 U.S.C. §112, first paragraph.

Whether claims 1, 7, 9, 11 and 12 were properly rejected under 35 U.S.C. §103(a) as obvious over Kinzer et al. (Kinzer), U.S. Patent No. 5,338,693 in view of Wang et al. (Wang).

Whether claims 3-6 and 13 were properly rejected under 35 U.S.C. §103(a) as obvious over Kinzer in view of knowledge in the art.

VII. ARGUMENT

A. Whether Claims 1, 3-7, 9 and 11-13 Were Properly Rejected

The Examiner has stated the following:

> Claims 1, 3, 7-9 and 11-13 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no description of a device wherein the gate oxide is "capable of withstanding damage due to single event effect that may cause a threshold voltage shift to -5 volts." There is only description of a device wherein the gate oxide resists damage due to particular events such that the resulting voltage shift is less than -5V.

The specification states that a device fabricated according to the present invention "maintains a threshold voltage of between -2V to -5V". (Spec., page 6, lines 13-16). As support, the specification discloses that a device fabricated according to the present invention did not

reach a threshold voltage of -5V after receiving 300 Krad of irradiation (spec., page 16, line 25 - page 17, line 2) and after an SEE (spec., page 17, lines 11-25). Thus, the specification discloses a device that does not suffer a shift to -5V threshold voltage (i.e. remains in between -2 and -5V).

It is respectfully submitted that the specification fully supports claim 1. Therefore, claim 1 complies with 35 U.SC. §112, first paragraph.

B. Whether Claim 1 was Properly Rejected Under 35 U.S.C. §103(a) over Kinzer in View of Wang

It has been asserted that Kinzer "does not disclose that the device is capable of resisting single event gate rupture due to single event effect. However, the device would have the recited property because it is the same device disclosed by applicant to exhibit such a property. Furthermore, no particular amount of 'resistance' is recited".

Claim 1, however, calls for P-channel device that includes a gate oxide that is less than 1000Å thick and "capable of withstanding damage due to total radiation does and capable of withstanding damage due to single event effect that may cause a threshold voltage shift to -5 volts."

Neither Kinzer nor Wang teaches or suggests a 1000Å thick gate oxide that can withstand damage due to total radiation dose and SEE which may cause a threshold voltage shift to -5 volts. Thus, claim 1 should not be deemed obvious over the combination of Kinzer and Wang.

Furthermore, Kinzer teaches doping the polysilicon that constitutes the gate electrodes thereof using a POCI process. As set forth in Kinzer, the deposition required for doping the polysilicon takes place at 925°C. Col. 6, lines 15-19.

On the other hand, in a device according to the present invention, the polysilicon constituting the gate electrodes of the device is doped through implantation. Thus, the gate dielectric is not exposed to a high temperature step, which as is well known, may adversely affect the ability of the same to withstand degradation due to cosmic radiation. Thus, it cannot be said that Kinzer discloses an identical device having identical characteristics as a device according to claim 1.

It is respectfully submitted that claim 1 should not be deemed obvious over the art of record.

C. Whether Claims 3-7, 9 and 11-13 were Properly Rejected

Claims 3-7, 9 and 11-13 depend from claim 1, and, therefore, include at least its limitations. Each of these claims includes other limitations, which in combination with those of claim 1, are not shown or suggested by the art of record. Claims 3-7, 9 and 11-13 should not, therefore, be deemed unpatentable over the art of record.

VIII. CONCLUSION

If this communication is filed after a shortened statutory time period has elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under 37 C.F.R. §1.136(a), to extend the time for filing a response to the outstanding Office Action by the number of months which will avoid abandonment under 37 C.F.R. §1.135. The fee under 37 C.F.R. §1.17 should be charged to our Deposit Account No. 15-0700.

In the event the actual fee is greater than the payment submitted or is inadvertently not enclosed or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 15-0700.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Appeal Brief - Patents, Commissioner of Patents and Trademarks, P.O. Box 1450, Alexandria, VA 22313-1450, on December 3, 2008

Kourosh Salehi
Name of applicant, assignee or Registered Representative

Signature

December 3, 2008
Date of Signature

Respectfully submitted,

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CLAIMS APPENDIX

1. A P-channel MOS gated device which is resistant to single event radiation failure and having improved total dose radiation resistance; said device comprising:

a P-type substrate having parallel upper and lower surfaces;

a plurality of laterally spaced N-type body regions extending from said upper surface into said substrate;

at least one respective P-type source region formed in each of said body regions in said upper surface of said substrate and defining a respective channel region in said upper surface in said N-type body region;

a gate electrode comprised of polysilicon implanted with p-type dopants disposed atop and insulated from said channel region and operable to invert said channel region in response to application of a suitable gate voltage to said gate electrode said gate electrode being insulated from said channel region by a gate oxide layer comprising silicon dioxide, said gate oxide layer being comprised of radiation hardened silicon dioxide and less than 1000Å thick;

an interlayer oxide disposed over each gate electrode and having tapered profile portions each aligned with a respective P-type source region; and

a source electrode disposed atop said upper surface and connected to said at least one P-type source region;

wherein said gate oxide is capable of withstanding damage due to total radiation dose and capable of withstanding damage due to a single event effect that may cause a threshold voltage shift to -5 volts.

2. (canceled).

3. The MOS gated device of claim 2 wherein said gate oxide layer has a thickness of between 500 to 1000Å.

4. The MOS gated device of claim 1 wherein each of said N-type body regions has a doping concentration corresponding to that of approximately 100 KeV phosphorus implant at a dose of about $5.5x10^{13}$ atoms/cm^2.

5. The MOS gated device of claim 1 wherein each of said N-type body regions has a doping concentration corresponding to that of approximately 100 KeV phosphorus implant at a dose of about $8.0x10^{13}$ atoms/cm^2.

6. The MOS gated device of claim 1 wherein said substrate includes a chip of monocrystalline silicon at said lower surface of said substrate and an epitaxial layer formed atop said chip that is less heavily doped than said chip.

7. The MOS gated device of claim 1 wherein at least one of said N-type body regions includes a portion adjacent to said upper surface that is more heavily doped than another portion of said N-type body region that is adjacent to a lower boundary between said N-type body region and said substrate.

8. (canceled).

9. The MOS gated device of claim 1 wherein said interlayer oxide is a low temperature oxide.

10. (canceled).

11. The MOS gated device of claim 1 further comprising a passivation layer formed atop said source electrode.

12. The MOS gated device of claim 11 wherein said passivation layer is comprised of low a temperature oxide.

13. The MOS gated device of claim 1 wherein said gate electrode has a doping concentration corresponding to that of approximately 50 KeV boron implant of about $5x10^{15}$ atoms/cm^2.

Claims 14-31 (canceled).

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.